University of Technology

Computer Engineering Department

Academic Year 2023 - 2024

Second Year – First Semester - All Branches



CE232	Computer Architecture I	2 Hours/Week	2 Units
Contents of Syllabus			Hours
• Register Transfer & Computer Organization: Data movement around registers. Data movement from/to memory, arithmetic and logic micro operations. Concept of bus and timing in register transfer.			4
• Basic Computer Organization: Computer Instructions, Timing and Control, Execution of Instructions, Design of Basic Computer.			6
• Microprogrammed Control Unit: Basic organization of microprogrammed control unit, Microinstruction formats, Address sequencer.			6
• CPU Organization: Addressing Modes, Instruction Format. CPU organization with large registers, stacks and handling of interrupts & subroutines.			6
• Arithmetic Processor Design: Addition subtraction for signed unsigned numbers and 2's complement numbers, Array multiplier, Booth's algorithm, Array divider.			4
	ocessing, Principle of pipelining, Instru azards of pipelining.	ction and arithmetic	6

References

- 1. Morrise Mano, "computer System architecture", 3rd Edition, Prentice Hall.
- 2. Mostara Abd-El-Barr, Hesham El-Rewini, "Fundamentals of Computer Organization and Architecture", John Wiley, 2005.
- 3. David A. Patterson, John L. Hennessy, "Computer Organization and Design", Arm Edition, Elsevier, 2010.

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