MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Systems Design**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☐**Lecture** ☒**Lab** ☒**Tutorial** ☒**Practical** ☐**Seminar**	
Module Code	**DISD124**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Type Dept. Code		**College**	Type College Code	
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Module Leader's Acad. Title	Assistant Prof.		**Module Leader's Qualification**	Ph.D.	
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Scientific Committee Approval Date	11/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	Logic Circuits Design	**Semester**	1
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. Learn how to use some of the exciting ICs to build digital circuits. 2. Learn how to verify the correctness of the design of logic circuits. 3. This course is essential for the Compute Architecture, Digital Communication and Microprocessor courses. 4. This course provides a systematic approach to digital design that can be applied to build various digital circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Reuse existing logic blocks to solve digital design problems. 2. Use different types of decoders to implement Boolean functions. 3. Understand the need for priority encoders. 4. Use multiplexers to implement Boolean functions and how to use a decoder IC as a demultiplexer. 5. Understand the usage of three-state gates. 6. Utilize PAL (Programmable Array Logic) to implement Boolean functions. 7. Understand the difference between sequential and combinational logic circuits and how feedback(s) can make a circuit to latch. 8. Differentiate between latches and flip-flops. 9. Understand how to build a flip-flop from latches and how to analyze a clocked sequential circuit. 10. Differentiate between Mealy and Moors models of finite state machines. 11. Apply a procedure to design clocked sequential circuits. 12. Understand how to build various types of shift registers. 13. Define the properties of shift register counters. 14. Build asynchronous counters and define their limitations. 15. Build synchronous counters using systematic design approach
Indicative Contents المحتويات الإرشادية	Indicative content includes the following: <u>Functions of Combinational Logic</u> Review of the procedure for designing logic circuits, binary multiplier, review of Verilog, decoders with active-HIGH enable and outputs ,decoders with active-LOW enable and outputs, implementing Boolean functions with decoders, cascading decoders, IC of 1 -of -16 decoder, gate-level description of decoders using Verilog, Binary Encoders, Priority encoders, the decimal to BCD Encoder, the decimal to BCD priority encoder, IC of decimal to BCD encoder, multiplexers, cascading multiplexers, IC of eight input data selector, implementing Boolean functions using multiplexers, demultiplexers, Behavioral description of multiplexers using Verilog ,IC 4-line to 16-line decoders as demultiplexers, three-state gates, multiplexers with three-state

	gates, Verilog model of three-state gates, PAL (programmable array logic), implementing SOP expressions using PAL, simplified notation for PAL diagrams, PAL general block diagram, basic types of PAL macrocells for combinational logic. [12 hrs] Introduction to Synchronous Sequential Logic Defining sequential circuits, latches, gated latches, describing latches using Verilog, edge triggered flip-flops, describing flip-flops using Verilog, master-slave flip-flop, flip-flop characteristics tables, flip-flip characteristics equations, analysis of clocked sequential circuits, state equations, state table, state diagram, flip-flop input equations, analysis with various types of flip-flops, Mealy and Moors models of finite state machines, state diagram-based Verilog model, design procedure for clocked sequential circuits, excitation tables of flip-flops, synthesis using various types of flip-flops, conversion of flip-flops [10 hrs] Registers Registers, shift registers, types of shift registers data inputs/outputs, shift register counters, Verilog model for registers. [4 hrs] Counters Asynchronous counters, up/down asynchronous counters, decade asynchronous counter, synchronous counters, design of synchronous counter, Verilog model for counters. [4 hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	These learning and teaching strategies aim to create an engaging and interactive learning environment. We summarize them below: 1. **Lectures:** the instructor will present in-class lectures to introduce and clarify important concepts, theories, and principles related to the design of digital logic circuits. 2. **Interactive Discussions**: Engaging students in interactive discussions to encourage critical thinking. 3. **Hands-on Laboratory Work**: students gain practical experience in a controlled environment to reinforce theoretical concepts. 4. **Group Projects:** Assigning group projects that require students to collaborate and work together to solve logic circuit design problems. This promotes teamwork, communication, and division of tasks. 5. **Simulations and Virtual Labs**: Utilizing simulation software and virtual labs to provide students with virtual hands-on experiences when physical resources are limited. 6. **Use of Visuals and Multimedia:** Incorporating visual aids, multimedia resources, and interactive tools can enhance understanding and

	engagement. 7. **Assessment and Feedback**: Regular assessments, including quizzes, tests, and examinations to show how well the students understand the subject. 8. **Practice and Revision Sessions**: Providing dedicated practice sessions and revision classes enables them to improve students' comprehension and strengthen their information.

Student Workload (SWL)

الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	7
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	6
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5 and 12	LO # 2, #4 and #10, #11
	Assignments	2	10% (10)	4 and 8	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	14	LO #4, #10 and #13
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #6
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Review of combinational logic circuit, binary multiplier logic circuit, review of Verilog
Week 2	Decoders, implementing Boolean functions using decoders, cascading decoders
Week 3	Encoders, Priority Encoders, Gate-level description of decoders and encoders using Verilog

Week 4	Multiplexers, cascading multiplexers, implementing Boolean functions using multiplexers, demultiplexers, Behavioral description of multiplexers using Verilog, demultiplexers
Week 5	Three-state gates, multiplexers with three-state gates, Verilog model of three-state gates
Week 6	PAL (programmable array logic), implementing SOP expressions using PAL, simplified notation for PAL diagrams, PAL general block diagram, basic types of PAL macrocells for combinational logic
Week 7	Mid-term Exam + Defining sequential circuits, latches, gated latches, describing latches using Verilog
Week 8	Edge triggered flip-flops, describing flip-flops using Verilog
Week 9	Master-slave flip-flop, flip-flip characteristics equations, state equations, state table, state diagram, flip-flop input equations, analysis with various types of flip-flops
Week 10	Mealy and Moors models of finite state machines, state diagram-based Verilog model
Week 11	Design procedure for clocked sequential circuits, excitation tables of flip-flops, synthesis using various types of flip-flops, conversion of flip-flops
Week 12	Registers, shift registers, Serial in/Serial out shift register, Serial in/Parallel out shift register, Parallel in/Serial out shift register, Parallel in/Parallel out shift register
Week 13	Ring counter, Johnson counter, Verilog model for registers
Week 14	Asynchronous counters, up/down asynchronous counters, decade asynchronous counter
Week 15	Synchronous counters, design of synchronous counter, Verilog model for counters
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Review of combinational logic circuit, binary multiplier logic circuit (using ALUs in Logisim)
Week 2	Lab 2: Decoders (implement 4:1 decoder and other decoder applications using Logisim)
Week 3	Lab 3: Encoders (implementation of encoder and some of its applications)
Week 4	Lab 4: Multiplexers(implementation of MUX with apps and utilizing MUX in design of Boolean functions)
Week 5	Lab 5: Demultiplexer (using Logisim to implement DEMUX and its applications)
Week 6	Lab 6: PAL (programmable array logic), implementing SOP expressions using PAL, simplified notation for PAL diagrams (in Logisim)
Week 7	Lab 7: Mid-Term Exam
Week 8	Lab 8: Sequential Logic cct (Latches in Logisim)
Week 9	Lab 9: Flip Flops implementation
Week 10	Lab 10: Flip Flops conversion

Week 11	Lab11: Design and implementation of Shift Registers (Serial)
Week 12	Lab 12: Design and implementation of Shift Registers (Parallel)
Week 13	Lab 13: Counters (Asynchronous-up)
Week 14	Lab 14: Counters (Synchronous-up)
Week 15	Lab 15:Counters (Synchronous and Asynchronous - Down)
Week 16	Review before final Exam

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	1-Digital Design with an Introduction to the Verilog, HDL, VHDL and System Verilog, Sixth edition, M. Morris Mano, Michael D. Ciletti, 2019. 2-Digital fundamentals, Eleventh Edition, Thomas L. Floyd, 2015.	NO NO
Recommended Texts		
Websites	https://www.coursera.org/learn/digital-systems	

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.