University of Technology

Computer Engineering Department

Academic Year 2023 - 2024





CE231	2 Units - 2 Hours Per Week
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Contents of Syllabus	Hours	
Synchronous sequential circuits.		
Basic definition.		
Analysis of sequential circuits.		
 Mealy machine and Moor machine. 		
 Design of synchronous sequential circuits. 	0.0	
Algorithmic state machines.	8h	
ASM chart.	1	
 Principal component of an ASM chart. 		
 Conversion of a state diagram to ASM chart. 		
 Design by using JK flip-flops, D flip-flops, one flip-flop per 		
state, multiplexers, and PLA		
Asynchronous sequential logic.		
 Analysis procedure - Derivation of primitive flow table. 		
Reduction of primitive flow table.	1	
• Cycles and races.		
• Hazards.		
Design examples		
Operational amplifiers.		
• Introduction.		
 Non-inverting Op-Amp. 		
• Inverting Op-Amp.		
 Voltage follower. 		
Voltage adder.		
• Integrator.		
• Differentiator.		
Differential. Input amplifier		
D/A and A/D Converters.		
 Variable resistor network. 		
• D/A converters.		
 Resistive divider DAC. 		
 Binary ladder DAC. 		
 DAC accuracy and resolution. 		
• A/D Converters.		

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Simultaneous ADC.		
Counter-type ADC.		
Continuous ADC.		
Successive approximation ADC		
Logic families (CMOS, TTL, ECL)	6h	
 Propagation delay, 		
• Switching speed limitations, power dissipation, fan-in/fan out constraints		
Programmable logic devices.	8h	
PLD advantages.		
ROM as PLD.		
PLA and PAL.		
Sequential programmable devices.		
Sequential PLD (SPLD).		
Complex PLD (CPLD).		
Field-Programmable Gate Array (FPGA).		
Generic array logic device (GAL).	V	
Mega PAL.		
Hard Array Logic (HAL).	1	
Introduction to VHDL.	8h	
The main features of VHDL.		
Design units.		
Structural modeling.		
Data flow modeling.		
Behavioral modeling.	1	
Mixed style of modeling.		
Concurrent vs Sequential.	11	
Components and Packages.		
Functions and procedures.		
VHDL simulation.		
VHDL synthesis		

References:

1.Shiv Shanker"Digital Circuit and Systems II ",2009

2. M. Morris Mano "Digital Design "four edition, 2007