University of Technology

Computer Engineering Department

Academic Year 2023 - 2024

Second Year – First Semester –Digital Electronics - All Branches

CE235	2 Units - 2 Hours Per Week

Contents of Syllabus	Hours
D/A and A/D Converters. • Variable resistor network. • D/A converters. • Resistive divider DAC. • Binary ladder DAC. • DAC accuracy and resolution. • A/D Converters. • Simultaneous ADC. • Counter-type ADC. • Continuous ADC. • Successive approximation ADC	8h
Logic families (CMOS, TTL, ECL) • Propagation delay, • Switching speed limitations, power dissipation, fan-in/fan out constraints	6h
Programmable logic devices. • PLD advantages. • ROM as PLD. • PLA and PAL. • Sequential programmable devices. • Sequential PLD (SPLD). • Complex PLD (CPLD). • Field-Programmable Gate Array (FPGA). • Generic array logic device (GAL). • Mega PAL. • Hard Array Logic (HAL).	8h
Introduction to VHDL. • The main features of VHDL. • Design units. • Structural modeling. • Data flow modeling. • Behavioral modeling. • Mixed style of modeling.	8h

• Concurrent vs Sequential. • Components and Packages. • Functions and procedures. • VHDL simulation. • VHDL synthesis	

References:

1.Shiv Shanker"Digital Circuit and Systems II " ,2009

2. M. Morris Mano "Digital Design "four edition , 2007